Z-Wave 800 SiP Module ZGM230S Errata

This document contains information on the ZGM230S errata. The latest available revision of this device is revision 2.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

Errata effective date: January, 2022.

1. Errata Summary

The table below lists all known errata for the ZGM230S and all unresolved errata in revision A0 of the ZGM230S.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:
			2
CUR_E302	Extra EM1 Current if FPU is Disabled	Yes	X
CUR_E303	Active AMUXCP Clock Causes High Current	Yes	X
DCDC_E302	DCDC Interrupts Block EM2/3 Entry or Cause Unexpected Wake-up	Yes	X
EMU_E305	DC-DC Refresh Time Delay	Yes	X
IADC_E305	FIFO Cannot Detect Eighth Entry	Yes	X
USART_E304	PRS Transmit Unavailable in Synchronous Secondary Mode	No	X

2. Current Errata Descriptions

2.1 CUR_E302 – Extra EM1 Current if FPU is Disabled

Description of Errata
When the Floating Point Unit (FPU) is disabled, the on-demand Fast Startup RC Oscillator (FSRCO) remains on after an energy mode transition from EM0 to EM1 is complete. This leads to higher current consumption in EM1.
Affected Conditions / Impacts
The enabled FSRCO increases EM1 current consumption by ~500 µA.
Workaround
Always enable the FPU at the beginning of code execution via the Coprocessor Access Control Register (CPACR) in the System Control Block (SCB) as shown below: `SCB->CPACR |= ((3 << 20) | (3 << 22));`
Resolution
There is currently no resolution for this issue.

2.2 CUR_E303 – Active AMUXCP Clock Causes High Current

Description of Errata
When the ACMP0, ACMP1, or IADC0 peripherals are active, the clock to the internal analog mux charge pump may also be activated, resulting in extra supply current.
Affected Conditions / Impacts
• ACMP0 and ACMP1: The charge pump clock is activated whenever either module is enabled via the ACMPn_EN_EN bit or when enabled by the LESENSE state machine. • IADC0: The charge pump clock is activated when any portion of the IADC analog circuitry is on. When IADC_CTRL_WARMUPMODE = KEEPINSTANDBY or KEEPWARM, the clock is activated as long as the IADC is enabled via the IADC_EN_EN bit. When IADC_CTRL_WARMUPMODE = NORMAL, the clock is activated only during warmup and conversion and will be shut down between conversions. • The extra current is from a shared block and increases supply current by an approximate total of 25 µA when any of the above conditions are true.
Workaround
No workaround exists to entirely eliminate the extra current. The impact of the current can be reduced by duty-cycling the peripheral. The average system supply current increase depends on the total percentage of time the peripheral(s) is/are active. For example, if only ACMP0 is used and enabled for 10% of the time, the average supply current increase is about 2.5 µA.
Resolution
This issue will be resolved in a future revision.

2.3 DCDC_E302 – DCDC Interrupts Block EM2/3 Entry or Cause Unexpected Wake-up

Description of Errata
Regardless of DCDC_IEN setting, if the DCDC interrupt is enabled in the NVIC, any of the four DCDC interrupt sources (DCDC_IF_WARM, DCDC_IF_RUNNING, DCDC_IF_TMAX, and DCDC_IF_BYPSW) can wake the device from EM2/3 or prevent it from entering EM2/3.
Affected Conditions / Impacts
The errata is limited to the DCDC_IF_WARM, DCDC_IF_RUNNING, DCDC_IF_TMAX and DCDC_IF_BYPSW requests, which also function as wake-up sources from EM2/3. When the NVIC DCDC interrupt source is enabled: • If IEN for one of these interrupt requests is set to 1 and that condition occurs, then an interrupt *will* occur and the CPU will branch to the DCDC IRQ handler. • If IEN for one of these interrupt sources is cleared to 0 and that condition occurs, then an interrupt *will not* occur. • If any of these four interrupt conditions occurs, regardless of the setting of their corresponding DCDC_IEN bits, the device *will* wake from EM2/3 and/or be prevented from entering EM2/3. If the corresponding IEN was not set, an interrupt *will not* occur even though the EM2/3 wakeup event has occurred.
Workaround
To prevent unwanted wake-up from or blocked entry into EM2/3, disable the DCDC interrupt using `NVIC_DisableIRQ(DCDC_IRQn)` before entering EM2/3 and re-enable the DCDC interrupt using `NVIC_EnableIRQ(DCDC_IRQn)` after EM2/3 wake-up.
Resolution
There is currently no resolution for this issue.

2.4 EMU_E305 – DC-DC Refresh Time Delay

Description of Errata
The DC-DC fast refresh delay required after exiting EM2/3 and entering continuous conduction mode (CCM) is not honored.
Affected Conditions / Impacts
When the system exits EM2/3 and the DC-DC is set to CCM, the DC-DC voltage comparator needs to be refreshed.This refresh delay is not honored when exiting EM2/3.
Workaround
Firmware must wait for at least 20 µs before enabling DCDC CCM upon wake from EM2/3.
Resolution
There is currently no resolution for this issue.

2.5 IADC_E305 – FIFO Cannot Detect Eighth Entry

Description of Errata
The IADC is unable to detect when the eighth FIFO entry has been loaded and will not set the corresponding SINGLEFIFODVL or SCANFIFODVL flag in the IADC_IF register or request LDMA service.
Affected Conditions / Impacts
If the DVL field of IADC_SINGLEFIFOCFG or IADC_SCANFIFOCFG is set to VALID8, a FIFO full condition is not registered when the eighth FIFO entry is loaded. In particular, this means that if the LDMA is configured to empty the FIFO when it is filled with eight entries, the LDMA will never issue a request to perform the transfers necessary to do this. Similarly, the IADC will not set the IADC_IF_SINGLEFIFODVL or IADC_IF_SCANFIFODVL to request an interrupt in response to the FIFO being filled with eight entries.
Workaround
Do not configure the IADC to request an interrupt or LDMA service when all eight entries are full (IADC_SINGLEFIFOCFG_DVL = VALID8 or IADC_SCANFIFOCFG_DVL = VALID8). All other settings of the DVL field (VALID1 to VALID7) operate as expected.
Resolution
There is currently no resolution for this issue.

2.6 USART_E304 — PRS Transmit Unavailable in Synchronous Secondary Mode

Description of Errata
When the USART is configured for synchronous secondary operation, the transmit output (MISO) is not driven if the signal is routed to a pin using the PRS producer (e.g., SOURCESEL = 0x20 and SIGSEL = 0x4 for USART0).
Affected Conditions / Impacts
Systems cannot operate the USART in synchronous secondary mode if the PRS is used to route the transmit output to the RX (MISO) pin. Operation is not affected in main mode when the transmit output is routed to the TX (MOSI) pin using the PRS producer nor is operation affected in any mode when the GPIO_USARTn_RXROUTE and GPIO_USARTn_TXROUTE registers are used.
Workaround
There is currently no workaround for this issue.
Resolution
There is currently no resolution for this issue.

3. Revision History

Revision 0.2

January, 2022

- Added CUR_E303.

Revision 0.1

December, 2021

- Initial release.

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