EZR32WG Errata

This document contains information on the EZR32WG errata. The latest available revision of this device is revision C.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from package marking or electronically.

Errata effective date: March 2021.

1. Errata Summary

The table below lists all known errata for the EZR32WG and all unresolved errata in revision C of the EZR32WG.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:		
			A	B	C
ADC_E118	Requirements for ADC_CLK > 7 MHz	Yes	X	X	X
BU_E105	LFXO Missing Cycles During IOVDD Ramping	Yes	X	X	X
CMU_E115	HFRCO 1 MHz Band Switching	Yes	X	X	X
DAC_E109	DAC Output Drift Over Lifetime	Yes	X	X	X
DMA_E102	2D Copy Corrupted by Ping-Pong or Scatter-Gather Operation on Another Channel	Yes	X	X	X
EMU_E110	Potential Hard Fault when Exiting EM2 or EM3	Yes	X	X	—
EZR_E101	Latched RSSI Feature May Not Work Properly	Yes	X	X	X
EZR_E102	Increased Harmonics in TX Mode When Using a Direct Tie Match	Yes	X	X	X
EZR_E103	LDC Mode Duty Cycling May Stop After First Packet Reception	Yes	X	X	X
EZR_E104	Auto RX Frequency Hop May Stop Hopping	Yes	X	X	X
EZR_E105	TX to TX Transition Timing May Vary	Yes	X	X	X
EZR_E106	RX Lock-Up May Occur When DSA is Enabled	Yes	X	X	X
EZR_E107	Sync Word Detection Timeout for Non-Standard Preamble May Not Work	Yes	X	X	X
EZR_E108	Invalid Sync Word Hardware Interrupt Prematurely Fires When Antenna Diversity is Enabled	Yes	X	X	X
EZR_E109	Radio Interface Speed	Yes	X	X	X
LES_E104	LFPRESC Can Extend Channel Start-Up Delay	Yes	X	X	X
PCNT_E102	PCNT Pulse Width Filtering Does Not Work	No	X	X	X
RMU_E101	POR Calibration Initialization Issue	Yes	X	X	—
RMU_E102	Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers	Yes	X	X	—
RMU_E103	Reset May Fail to Trigger During Supply Voltage Brownouts	Yes	X	X	—
TIMER_E103	Capture/Compare Output is Unreliable with RSSCOIST Enabled	No	X	X	X
USART_E113	IrDA Modulation and Transmission of PRS Input Data	Yes	X	X	X
USB_E103	HNP Sequence Fails if A-Device Connects After 3.4 ms	No	X	X	X
USB_E104	USB A-Device Delays the HNP Switch Back Process	No	X	X	X
USB_E105	B-Device as Host Driving K-J Pairs During Reset	No	X	X	X
USB_E109	Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1	Yes	X	X	X
USB_E110	Unexpected USB_HCx_INT.CHHLTD Interrupt	Yes	X	X	X

2. Current Errata Descriptions

2.1 ADC_E118 — Requirements for ADC_CLK > 7 MHz

Description of Errata
If operating the ADC_CLK at frequencies greater than 7 MHz, the ADC_BIASPROG register default value of 0x747 may not be sufficient to achieve the published missing codes performance specification.
Affected Conditions / Impacts
Devices operating the ADC_CLK at frequencies greater than 7 MHz while using the default ADC_BIASPROG value of 0x747 may experience performance outside data sheet limits.
Workaround
For systems requiring an ADC_CLK rate > 7 MHz, it may be necessary to increase the ADC's bias current components via the COMPBIAS, BIASPROG, and/or HALFBIAS bit fields in the ADC_BIASPROG register depending on a given application's ADC performance requirements.
Resolution
There is currently no resolution for this issue.

2.2 BU_E105 — LFXO Missing Cycles During IOVDD Ramping

Description of Errata
LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.
Affected Conditions / Impacts
When IOVDD is ramped, the dc-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.
Workaround
Set PRESC in BURTC_CTRL to greater than 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
Resolution
There is currently no resolution for this issue.

2.3 CMU_E115 — HFRCO 1 MHz Band Switching

Description of Errata
Switching to or from the 1 MHz band of the HFRCO or AUXHFRCO may cause a hard fault even at the maximum supported number of wait states.
Affected Conditions / Impacts
When the HFRCO or AUXHFRCO is selected as a clock source (e.g., the HFRCO has been selected as the HFCLK source) and the device is running with the maximum supported number of wait states, switching to or from the 1 MHz band can possibly cause a clock glitch that results in unexpected behavior or a hard fault.
Workaround
Before switching to or from the 1 MHz band when the HFRCO or AUXHFRCO is selected as the clock source, first switch to another stable clock source (such as the LFRCO). For example, when switching from the 21 MHz band to the 1 MHz band, the following procedure needs to be followed: 1. Select another stable clock source by writing to the HFCLKSEL field of the CMU_CMD register. 2. Wait until the clock source shows that it has been selected in the CMU_STATUS register, (e.g., CMU_STATUS_LFRCOSEL = 1). 3. Program the CMU_HFRCOCTRL register to select the 1 MHz band and tuning value. 4. Wait until the HFRCO has stabilized at the new frequency by waiting for the HFRCORDY bit in the CMU_STATUS register to change for 0 to 1. 5. Select the HFRCO as the clock source by writing to the HFCLKSEL field of the CMU_CMD register.
Resolution
There is currently no resolution for this issue.

2.4 DAC_E109 — DAC Output Drift Over Lifetime

Description of Errata
The voltage output of the DAC might drift over time.
Affected Conditions / Impacts
When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur.
Workaround
Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect.
Resolution
There is currently no resolution for this issue.

2.5 DMA_E102 — 2D Copy Corrupted by Ping-Pong or Scatter-Gather Operation on Another Channel

Description of Errata
When performing a 2D copy (rectangular copy) on one DMA channel, more data than is specified is occasionally transferred from the source buffer if another channel is being used in ping-pong or scatter-gather mode.
Affected Conditions / Impacts
The incorrect number of bytes is transferred during the 2D copy when there is corruption caused by concurrent ping-pong or scatter-gather operation. This would be most noticeable when 2D copy is used for moving a graphic image to a display but could cause problems in other use cases.
Workaround
Do not allow ping-pong or scatter-gather mode DMA transfers to occur concurrently with a 2D copy. If both types operations are required, interleave them such that the 2D copy is complete before enabling a channel in ping-pong or scatter-gather mode or vice versa.
Resolution
There is currently no resolution for this issue.

2.6 EZR_E101 — Latched RSSI Feature May Not Work Properly

Description of Errata
The Latched RSSI may not be captured properly if the latching instant is based on Tbit/Tsample.
Affected Conditions / Impacts
The Latched RSSI may not be captured properly if the latching instant is based on Tbit/Tsample. In other words, when MODEM_RSSI_CONTROL: Latch = RX_STATE1-RX_STATE5, or MODEM_RSSI_CONTROL: AVERAGE = Sample1 the returned Latched RSSI may be invalid.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.7 EZR_E102 — Increased Harmonics in TX Mode When Using a Direct Tie Match

Description of Errata
In TX mode, harmonic content may be excessive due to incorrect LNA configuration when using a direct tie match. Increase of the 3rd harmonic can be as high as 20 dB.
Affected Conditions / Impacts
Increased harmonics levels in the TX spectrum. No impact when operating in RX state or when using a split TX / RX match or a match with an RF switch and single antenna. Both EZRadio and EZRadioPRO parts are affected.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.8 EZR_E103 — LDC Mode Duty Cycling May Stop After First Packet Reception

Description of Errata
When LDC (Low Duty Cycling) mode is enabled, the radio may stop receiving packets after the first successfully received packet.
Affected Conditions / Impacts
The chip may stop entering RX state autonomously. Only EZRadioPRO parts are affected.
Workaround
There are two workarounds available. 1. After reading the RX FIFO, enter Sleep state. 2. Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.9 EZR_E104 — Auto RX Frequency Hop May Stop Hopping

Description of Errata
Without any signal present, the radio may stop hopping after a while and stay in receive mode at a seemingly random channel.
Affected Conditions / Impacts
Automatic frequency hopping may stop working. The device is still functional and will respond to subsequent commands from the host. Only EZRadioPRO parts are affected.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.10 EZR_E105 — TX to TX Transition Timing May Vary

Description of Errata
RevC2A chips support TX to TX state transitions, however, the amount of time it takes to do so may be inconsistent.
Affected Conditions / Impacts
TX to TX state transition time may vary. Both EZRadio and EZRadioPRO parts are affected. This does not affect the manual TX_HOP timing.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.11 EZR_E106 — RX Lock-Up May Occur When DSA is Enabled

Description of Errata
RevC2A chips have a new block, Digital Signal Arrival detector (DSA), which can be used to detect preamble in a very short period of time. The DSA is used for Preamble Sense Mode (PSM) amongst other features, where the chip duty cycles between RX Idle and RX state while searching for a preamble. When the DSA is enabled an RX lock-up may occur.
Affected Conditions / Impacts
RX lock-up may occur. The device is still functional and will respond to subsequent commands from the host. Only EZRadioPRO parts are affected.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.12 EZR_E107 — Sync Word Detection Timeout for Non-Standard Preamble May Not Work

Description of Errata
It is possible to configure the device for non-standard preamble (i.e. other than a 1010, or a 0101 pattern), in which case the sync word timeout is controlled by the packet handler. When this feature is enabled, the sync word detection timeout may not work correctly.
Affected Conditions / Impacts
Without a sync word timeout, the chip may continue searching for a sync word instead of going back to searching for non-standard preamble. No impact if standard preamble is used. Only EZRadioPRO parts are affected.
Workaround
Apply patch (Patch ID: 0x311A).
Resolution
Apply the patch (Patch ID: 0x311A) to resolve this problem.

2.13 EZR_E108 — Invalid Sync Word Hardware Interrupt Prematurely Fires When Antenna Diversity is Enabled

Description of Errata
If Invalid Sync Word hardware interrupt is enabled, it may fire right after PREAMBLE_VALID signal without receiving enough number of bits to determine whether or not there is a Sync Word pattern match.
Affected Conditions / Impacts
Invalid Sync Word detect NIRQ hardware interrupt cannot be used when Antenna Diversity is enabled. Only EZRadioPRO parts are affected.
Workaround
Disable Invalid Sync Word detect NIRQ hardware interrupt when Antenna Diversity is enabled.
Resolution
There is currently no resolution for this issue.

2.14 EZR_E109 — Radio Interface Speed

Description of Errata
The USART interface between the radio and MCU is set to run at 8 MHz, and no communication issues have been observed at this speed. However, this speed may violate some of the data sheet specifications for either the MCU or radio. A future version of the stack software will address this by slightly reducing the USART interface speed.
Affected Conditions / Impacts
There are currently no impacts as a result of this issue, as no communication issues have been observed as a result of the 8 MHz interface speed.
Workaround
There is currently no workaround for this issue.
Resolution
There is currently no resolution for this issue.

2.15 LES_E104 — LFPRESC Can Extend Channel Start-Up Delay

Description of Errata
Setting LESENSE_TIMCTRL_LFPRESC to a value other than DIV1 may delay channel start-up longer than the number of $LFACLK_{LESENSE}$ clock cycles specified by LESENSE_TIMCTRL_STARTDLY.
Affected Conditions / Impacts
Delaying channel start-up delays the subsequent excitation and measurement phases and may have an impact on the data returned by the LESENSE.
Workaround
If a channel start-up delay is used (LESENSE_TIMCTRL_STARTDLY > 0), LESENSE_TIMCTRL_LFPRESC must be set to DIV1.
Resolution
There is currently no resolution for this issue.

2.16 PCNT_E102 — PCNT Pulse Width Filtering Does Not Work

Description of Errata
PCNT pulse width filtering does not work.
Affected Conditions / Impacts
The PCNT pulse width filter does not work as intended.
Workaround
Do not use the pulse width filter, i.e., ensure FILT = 0 in PCNTn_CTRL.
Resolution
There is currently no resolution for this issue.

2.17 TIMER_E103 — Capture/Compare Output is Unreliable with RSSCOIST Enabled

Description of Errata
The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.
Affected Conditions / Impacts
When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.
Workaround
Do not use a prescaled clock, i.e., ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.
Resolution
There is currently no resolution for this issue.

2.18 USART_E113 — IrDA Modulation and Transmission of PRS Input Data

Description of Errata
If the USART IrDA modulator is configured to accept input from a PRS channel, the incoming data stream will not be transmitted because the required clock from the baud rate generator is never enabled.
Affected Conditions / Impacts
It is not possible for the USART IrDA modulator to directly transmit data from a source other than the USART's own transmitter. The USART_IRCTRL_IRPRSEN bit should remain at its reset state of 0.
Workaround
Assuming the data to be sent via the PRS is also data that could be received by the EFM32/EFR32 USART, then the data can be received using the USART's PRS RX feature (USART_INPUT_RXPRS = 1), stored in RAM (e.g., using DMA), and then transmitted with IrDA mode enabled. In cases where IrDA operation is transmit-only, the PRS RX data can be received on the same USART doing the transmission. If IrDA operation is bidirectional, then another USART must be used to receive the PRS data. If the data to be sent is in some other format (e.g., pulses from a timer output), then there is no direct way to transmit it using the IrDA modulator. It would be necessary to capture the data in some other way and reformat it as serial data timed according to the clock generated by the USART.
Resolution
There is currently no resolution for this issue.

2.19 USB_E103 — HNP Sequence Fails if A-Device Connects After 3.4 ms

Description of Errata
HNP Sequence fails if A-Device connects after 3.4 ms.
Affected Conditions / Impacts
The B-Device core only waits for up to 3.4 ms before signalling HNP fail and reverting back to Peripheral mode. Therefore, the HNP sequence fails if the A-Device connects after 3.4 ms.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.20 USB_E104 — USB A-Device Delays the HNP Switch Back Process

Description of Errata
The D+ line disconnects after 200 ms, delaying the HNP switch back process.
Affected Conditions / Impacts
The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the other side of the USB pipe either should wait for disconnect from the A-Device or should switch to Peripheral mode and wait for the A-Device to issue a USB reset. Hence, there is no significant impact on actual operation.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.21 USB_E105 — B-Device as Host Driving K-J Pairs During Reset

Description of Errata
The A-Device misinterprets the K-J pairs as Suspend after switching to High Speed mode.
Affected Conditions / Impacts
If the B-Device as Host on the other side of the USB pipe drives K-J pairs for more than 200 ms during USB reset, the A-Device core exits peripheral state, causing the HNP process to fail. There is no significant impact since normally the host drives USB reset for a shorter time than 200 ms.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.22 USB_E109 — Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1

Description of Errata
A Host-initiated Suspend, followed by a Host Disconnect and Host Connect, will not result in a SessReq interrupt.
Affected Conditions / Impacts
When USB_PCGCCTL.STOPPCLK is set and the device is acting as a B-peripheral, a Host-initated Suspend, followed by a Host Disconnect and Host Connect, will not result in a SessReq interrupt.
Workaround
If this is an expected use-case, USB_PCGCCTL.STOPPCLK should not be set. USB_PCGCCTL.GATEHCLK can still be used to save power.
Resolution
There is currently no resolution for this issue.

2.23 USB_E110 — Unexpected USB_HCx_INT.CHHLTD Interrupt

Description of Errata
In some cases the USB_HCx_INT.CHHLTD interrupt might be incorrectly set.
Affected Conditions / Impacts
In some cases, an unexpected USB_HCx_INT.CHHLTD interrupt might be received from another endpoint that does not have the USB_HCx_CHAR.CHDIS, USB_HCx_INT.XACTERR, USB_HCx_INT.BBLERR, USB_HCx_INT.DATATGLERR, or USB_HCx_INT.XFERCOMPL interrupts enabled.
Workaround
If such an interrupt is received, the application must re-enable the channel for which it received the unexpected USB_HCx_INT.CHHLTD interrupt.
Resolution
There is currently no resolution for this issue.

3. Resolved Errata Descriptions

This section contains previous errata for EZR32WG devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 EMU_E110 — Potential Hard Fault when Exiting EM2 or EM3

Description of Errata
The flash is powered down in EM2 and EM3 to save power. Some control registers in the flash can rarely enter an invalid state upon power-on, causing the first read of flash to be incorrect. If this occurs after exiting EM2 or EM3, the core attempts to fetch the interrupt address, but the value will be incorrect and may be invalid. In the case of an invalid value, the core will then jump to the hard fault handler for attempting to execute code from an invalid address. All subsequent reads from the flash are unaffected, and it is only the first flash read after exit from EM2 or EM3 that is potentially erroneous.
Affected Conditions / Impacts
When exiting EM2 or EM3, some devices may intermittently execute code incorrectly or enter the hard fault handler instead of entering the expected ISR associated with the wake source.
Workaround
To workaround this issue, move the interrupt vector table and interrupt service routines for EM2 or EM3 wake sources to RAM and perform a dummy read of the flash in the ISR. Additional information on the workaround and examples provided is available from the following Knowledge Base article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2017/05/09/emu_e110_-_potential-i2Pn
Resolution
This issue has been resolved. Devices with a date code greater than or equal to 1742 will not have this issue.

3.2 RMU_E101 — POR Calibration Initialization Issue

Description of Errata
Upon initial power-on, some devices may not be able to access flash memory above the 4 kB boundary, or some calibration registers on some devices may not be set to their factory calibration values.
Affected Conditions / Impacts
The list of affected devices can be found in the Knowledge Base (KB) article listed under Fix/Workaround. Some devices are sensitive to the power supply ramp during initial power-on. Specific ramp profiles on these devices can cause an intermittent issue resulting in one of two failure modes (A) or (B): A. Flash memory above the 4 kB boundary is inaccessible. Reads of the flash will return zeros. Write attempts will return an invalid address error code in the MSC_STATUS register. Code execution will behave as though the memory above 4 kB was filled with zeros until the device resets itself. B. Some parts of the calibration initialization process do not complete successfully. On USB devices, the USB voltage regulator does not get calibrated. Specific peripheral registers that may not be calibrated are as follows (not all registers apply to all devices): ADC0_CAL, IDAC_CAL, DAC0_CAL, DAC0_BIASPROG, DAC0_OPACTRL, and DAC0_OPAOFFSET. A SYSRESETREQ reset will clear either failure mode, and the device will behave normally until the next power-on event.
Workaround
Additional information including a software workaround is available from the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2015/10/09/rmu_e101_-_por_calib-cEpZ
Resolution
This issue has been resolved. Devices with a date code and PROD_REV greater than or equal to 1537 and 0x88, respectively, will not have this issue.

3.3 RMU_E102 — Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers

Description of Errata
Output of the on-chip regulator (DECOUPLE pin) may be approximately 0 V, and the device will not respond to a pin reset.
Affected Conditions / Impacts
The device supply voltage is specified as 1.98 V minimum. For certain supply waveforms, similar to disconnecting a battery, allowing the supply to decay to approximately 0.9 V (and stopping the decay at approximately 0.9 V), then reconnecting the battery, the output of the regulator (DECOUPLE pin) may be approximately 0 V. In this state, code will not execute, and the device will not respond to a pin reset. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e102_por_bodres-AQh7
Workaround
Hold the RESETn pin logic low, starting before the supply is disconnected, and keep RESETn pin logic low until the supply reaches a valid voltage. If the DECOUPLE pin measures approximately 0 V, power cycle the supplies by pulling them all the way to 0 V before connecting supplies again.
Resolution
This issue is resolved in revision C devices.

3.4 RMU_E103 — Reset May Fail to Trigger During Supply Voltage Brownouts

Description of Errata
Reset may fail to trigger when the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range.
Affected Conditions / Impacts
If the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range, the device may fail to reset, allowing code execution while the supply voltage remains in the 1.25 - 1.45 V range. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e103_por_bodres-N3MD
Workaround
Hold the RESETn pin in logic low, starting before the device supplies fall below 1.6 V, and keep the RESETn pin logic low until the device supplies reach a valid voltage again.
Resolution
This issue is resolved in revision C devices.

4. Revision History

Revision 1.40

March, 2021

- Added CMU_E115

Revision 1.30

November, 2019

- Updated to product revision C.
- Added ADC_E118 and LES_E104.
- Resolved RMU_E102 and RMU_E103.
- Migrated to new errata document format.

Revision 1.20

January, 2019

- Added DMA_E102, EZR_E109, RMU_E102, RMU_E103, and USART_E113.
- Resolved EMU_E110 and updated language to refer to both EM2 and EM3.
- Revision C removed from RMU_E101 resolution and workaround URL updated.

Revision 1.10

April, 2017

- Added EMU_E110.
- Updated errata formatting.
- Merged all errata documents for EZR32WG devices into one document.
- Merged errata history and errata into one document.
- Updated to revision B.

Revision 1.00

October, 2015

- Initial preliminary release.

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